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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,380	01/22/2007	Takashi Hasunuma	YH0018-US1	6606

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EXAMINER	
MURALIDAR, RICHARD V	

ART UNIT	PAPER NUMBER
2858	

MAIL DATE	DELIVERY MODE
09/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,380	HASUNUMA ET AL.	
	Examiner	Art Unit	
	RICHARD V. MURALIDAR	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,10 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,10 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to applicant's reply received 6/23/2009. Claims 1 and 4 are amended. Dependent claims 3, 8, and 9 have been cancelled by applicant. Claims 1, 2, 4-7, 10 and 11 are pending for examination below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. **Claims 1, 2, 4-7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda [U.S. 6,963,477] in view of Myong et al. [U.S. 6,356,424].**

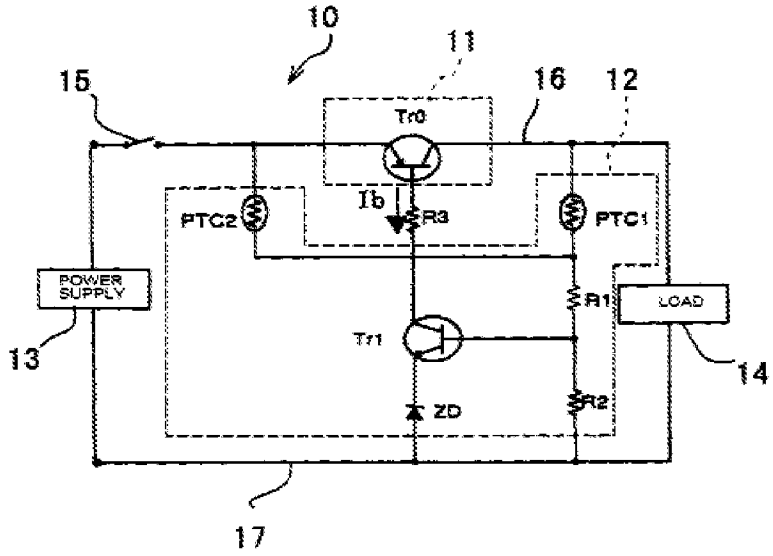
4. With respect to claim 1, Ikeda discloses an overheat protection device [see Ikeda's Fig. 1 reproduced below] comprising a variable resistive element [Fig. 1; PTC1] for of which resistance varies depending on a temperature and which is a PTC element

[Fig. 1; PTC1 element; col. 5 lines 7-9], characterized in that the device further comprises a switching element [Fig. 1; 11; transistor Tr0] which controls a current flowing through an electrical system [Fig. 1; power supply 13] depending on an applied voltage thereto [col. 4 lines 59 – col. 5 lines 6], and the variable resistive element [Fig. 1, PTC1] is located on and thermally combined with a certain position of the electrical system [Fig. 1; power supply 13] and interrupts the current flowing through the electrical system by changing the applied voltage to the switching element when the certain position comes to be under a high temperature condition [col. 5 lines 6 – col. 7 lines 20].

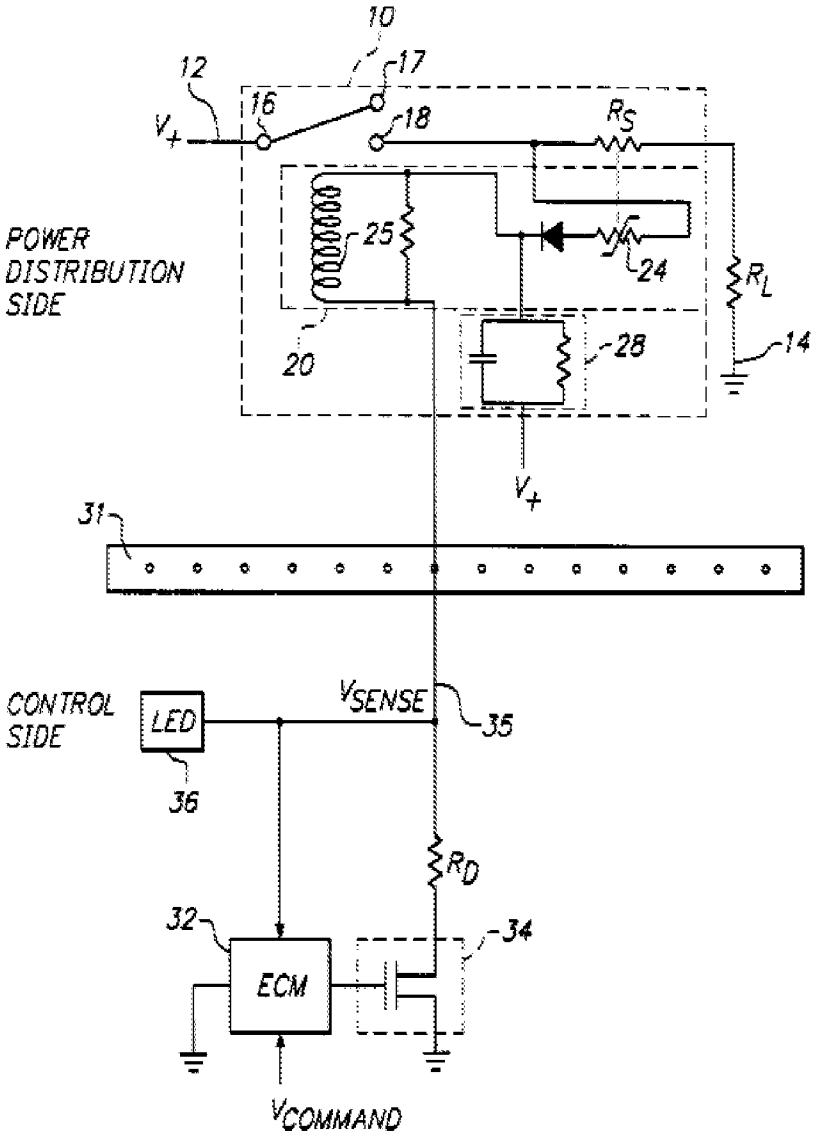
5. Ikeda does not disclose that the PTC element is a polymer PTC element.

6. Myong discloses an electrical protection system having control elements in series with a PTC device [see Myong's Fig. 1 reproduced below; PTC 24]. Myong discloses a PTC element that is a polymer PTC element [col. 1 lines 29-46; col. 4 lines 46-61].

7. Ikeda and Myong are analogous electrical protection circuits that use PTC elements. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the polymer PTC element, as taught by Myong, with Ikeda's protection circuit for the benefits of higher resistivity and their known advantages over ceramic PTC elements for protecting batteries from excessive currents and temperatures [Myong col. 1 lines 35-46].



Ikeda's Fig. 1 [U.S. 6963477] showing PTC 1



Myong's Fig. 1 [U.S. 6356424] showing polymer PTC 24

8. With respect to claim 2, Ikeda disclose that the electrical system comprises a secondary battery [Fig. 2; power supply 13 is a battery; col. 4 lines 56-58], and the variable resistive element [Fig. 1; PTC1] is located on and thermally combined with the secondary battery.

9. With respect to claim 4, Ikeda discloses that the variable resistive element is a PTC element, but does not disclose that the variable resistive element is composed of a

plurality of variable resistive elements, which are electrically connected in series with each other.

10. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided the circuit with either one or more of a plurality of variable resistive elements for the purpose of increasing or decreasing the PTC temperature threshold (i.e. varying the ON/TRIP threshold as desired). Additionally, it has been held that mere duplication of the essential working parts of a device (in this case, placing multiple PTC elements in series with each other) involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

11. With respect to claim 5, Ikeda further comprises a resistor [Fig. 1; R2], the variable resistive element [Fig. 1; PTC1] and the resistor [Fig. 1; R2] are electrically connected in series with each other and in parallel to the electrical system [Fig. 1; PTC1 and R2 are in parallel with the power supply 13], and the switching element [Fig. 1; Tr0, Tr1] is electrically connected in parallel to the resistor.

12. With respect to claim 6, Ikeda discloses that the switching element [Fig. 1; transistors Tr0 and Tr1] is a field effect transistor (FET) [col. 8 lines 62-65], a gate of the FET is electrically connected to a position between the variable resistive element and one end of the resistor [Fig. 1; the gate of transistor Tr0 is connected between the PTC1 and resistor R2], a source of the FET is electrically connected to another end of the resistor [Fig. 1; source of transistor Tr0 is connected to another end of resistor R2 via PTC1], the source and a drain of the FET are electrically connected to form a part of an electric circuit comprising the electrical system [Fig. 1; the source and the drain of transistor Tr0 are electrically connected], and when a voltage between the

gate and the source of the FET [Fig. 1; transistor Tr0] becomes not greater than a threshold value, the current does not substantially flow between the source and the drain of the FET so that the current flowing through the electrical system is interrupted [this is the normal operation of the transistor].

13. With respect to claim 7, Ikeda discloses that a value of the voltage between the gate and the source is expressed as a following formula (1): Vgs = Vo * (R/(P+R)); wherein the Vgs is the voltage between the gate and the source, the V0 is a voltage across the variable resistive element and the resistor, the P is a resistance of the variable resistive element, and the R is a resistance of the resistor [This is the standard voltage divider formula for calculating voltage across the gate and the source of the transistor. One of ordinary skill in the art would know how to apply this to Fig. 1 of Ikeda in order to determine the applicable Vgs].

14. With respect to claim 10, Ikeda discloses an electrical system comprising the overheat protection device according to claim 1 [col. 1 lines 5-10].

15. With respect to claim 11, Ikeda discloses that the electrical system comprises a secondary battery [Fig. 1; power supply 13; col. 4 lines 56-58] which is electrically connected to an electrical element [Fig. 1; source and drain of transistor Tr0] to form an electric circuit, and the overheat protection device [Fig. 1; PTC1 and resistors R1, R2] is connected in parallel to and between the secondary battery and the electrical element [as shown in Fig. 1].

Response to Arguments

16. Applicant's arguments with respect to claims received 06/23/2009 have been considered but are moot in view of the new ground(s) of rejection. Any arguments with respect to amended claims have been addressed in the action above.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD V. MURALIDAR whose telephone number is (571)272-8933. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick J. Assouad can be reached on 571-272-2210. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Richard V Muralidar/
Examiner, Art Unit 2858

/Patrick J Assouad/
Supervisory Patent Examiner, Art Unit 2862